Customer No.: 31561
Application No.: 10/709,090
Docket No.:12029-US-PA

REMARKS

Present Status of the Application

The outstanding Office Action rejected all presently-pending claims 1-22. Specifically, the Office Action rejected claims 1-3, 5-10, 12-14 and 17-22 under U.S.C. 102(e) as being anticipated by US 6,894,736B2 (*Chae*) and the Office Action also rejected claims 4, 11 and 15-16 under U.S.C. 103(a) as being unpatentable over *Chae* in view of US 5,734,449 (*Jang*). Applicants have amended claims 1, 10 and 22 to more explicitly describe the present invention. Claims 1-22 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Discussion of Double Patenting

Regarding to the Double Patenting issue, Applicants is submitting a terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) to render the rejection moot.

Discussion of Office Action Rejections

1. The Office Action rejected claims 1-3, 5-10, 12-14 and 17-22 under U.S.C. 102(e) as being anticipated by US 6,894,736B2 (*Chae*). Applicants respectfully traverse the rejections for at least the reasons set forth below.

Independent claim 1 recites the features as follows:

1. A pixel structure, comprising:

a scan line, disposed over a substrate;

a data line, disposed over the substrate;

an active component, disposed over the substrate adjacent to an intersection of the scan line and the data line, wherein the active component is electrically connected to the scan line and the data line;

a plurality of transparent capacitance electrodes, disposed over the substrate, wherein the transparent capacitance electrodes comprises at least a first transparent capacitance electrode and at least a second transparent capacitance electrode disposed above the first transparent capacitance electrode; and

a pixel electrode, ***electrically connected to the first transparent capacitance electrode and the active component, wherein at least a first pixel storage capacitor is formed between the first transparent capacitance electrode and the second transparent capacitance electrode, and at least a second pixel storage capacitor parallel connected to the first pixel storage capacitor is formed between the second transparent capacitance electrode and the pixel electrode***.

(Emphasis added).

Claims 2-9 also recite the similar features.

Independent claim 10 recites the features as follows:

10. A manufacturing method, for a pixel structure, comprising:

sequentially forming an active component, a scan line and a data line over a substrate, wherein the active component is electrically connected to the scan line and the data line;

forming a plurality of transparent capacitance electrodes over the substrate, wherein the transparent capacitance electrodes comprises at least a first transparent capacitance electrode and at least a second transparent capacitance electrode formed above the first transparent capacitance electrode; and

forming a pixel electrode over the transparent capacitance electrodes, wherein the pixel electrode is electrically connected to the active component, wherein ***at least a first pixel storage capacitor is formed between the first transparent capacitance electrode and the second transparent capacitance electrode, and at least a second pixel storage capacitor parallel connected to the first pixel storage capacitor is***

formed between the second transparent capacitance electrode and the pixel electrode.

(Emphasis added).

Claims 11-19 also recite the similar features.

Independent claim 20 recites the features as follows:

20. A pixel structure, comprising:
a scan line, disposed over a substrate;
a data line, disposed over the substrate;
an active component, disposed over the substrate adjacent to an intersection of the scan line and the data line, wherein the active component is electrically connected to the scan line and the data line;
a first transparent capacitance electrode, disposed over the substrate;
a pixel electrode, disposed over the first transparent capacitance electrode and electrically connected to the active component and the first transparent capacitance electrode; and
a second transparent capacitance electrode, disposed between the first transparent capacitance electrode and the pixel electrode, wherein a multilayer pixel storage capacitor is formed by the pixel electrode, the first transparent capacitance electrode and the second transparent capacitance electrode.

(Emphasis added).

Claim 21 also recite the similar features.

Independent claim 22 recites the features as follows:

22. A pixel structure, comprising:
a scan line, disposed over a substrate;
a data line, disposed over the substrate;
an active component, disposed over the substrate adjacent to an intersection of the scan line and the data line, wherein the active component comprises a gate electrically connected to the scan line, a channel disposed over the gate and a source/drain disposed over the channel and electrically connected to the data line and the pixel electrode;
a protection layer, disposed over the substrate for covering the gate of the active component;
a plurality of transparent capacitance electrodes, disposed over the substrate, the transparent capacitance electrodes comprising at least a first transparent capacitance electrode and at least a second transparent capacitance electrode disposed above the first transparent capacitance electrode, wherein the first transparent capacitance electrode is disposed on the protection layer; and
a pixel electrode, ***electrically connected to the first transparent capacitance electrode and the active component, wherein at least a first pixel storage capacitor is formed between the first transparent capacitance electrode and the second transparent capacitance electrode, and at least a second pixel storage capacitor parallel connected to the first pixel storage capacitor is formed between the second transparent capacitance electrode and the pixel electrode***.

In re FIG. 5A, 5B, 6A, 6B and related contents disclosed by *Chae*, Applicants consider that *Chae* fails to disclose "***the first pixel storage capacitor and the second pixel storage capacitor parallel connected to the first pixel storage capacitor***" and "***a second transparent capacitance electrode disposed between the first transparent capacitance electrode and the pixel electrode***" as recited in independent claims 1, 10, 20 and 22. Therefore, Applicants consider that claims 1-22 meet the requirement of novelty and the 102(e) rejection should be withdrawn.

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2. The Office Action rejected claims 1, 10 and 22 under 35 U.S.C. 103(a), as being unpatentable over *Chae* in view of US 5,734,449 (*Jang*). Applicants respectfully traverse the rejections for at least the reasons set forth below.

In re FIG. 5A, 5B, 6A, 6B and related contents of US 5,734,449, *Chae* merely disclosed a pixel having single capacitor therein. Specifically, the capacitor of the pixel is constituted by the capacitor lower electrode 59a, the gate insulating film 52 and the capacitor upper electrode 59b (FIG. 5B), or constituted by the capacitor lower electrode 69a, the gate insulating film 62 and the capacitor upper electrode 69b (FIG. 6B). It is noted that, the pixel electrode 56 or 66 is not electrically connected with the capacitor lower electrode 59a or 69a, which is located under the capacitor upper electrode 59b or 69b. Obviously, there is only one capacitor in the pixel disclosed by *Chae* and the capacitance of the capacitor disclosed by *Chae* is limited. On the contrary, in the pixel structure recited in claims 1, 10 and 22, ***the first pixel storage capacitor*** and ***the second pixel storage capacitor parallel connected to the first pixel storage capacitor*** is capable of increasing the overall the capacitance of the pixel structure without degrading aperture ratio. Accordingly, flexibility of layout design can be improved by the present invention significantly. Therefore, the features related to "***the first pixel storage capacitor***" and "***the second pixel storage capacitor parallel connected to the first pixel storage capacitor***" are non-obvious.

Therefore, Applicant considers that Claims 1, 10 and 22 are patently distinguished from US Patent No. 5,734,449.

In the claimed invention, the aperture ratio is not affected by the area occupied by the storage capacitor (i.e. area of transparent capacitance electrodes) even the transparent capacitance electrodes of the storage capacitor occupy almost region under the pixel electrode.

According to MPEP 2143.03 (All Claim Limitations Must Be Taught or Suggested), Applicants think that "to establish prima facie obviousness of a claimed invention, **all the claim limitations must be taught or suggested by the prior art**. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974)", however, *Jang and Chae* **failed to disclose** "***the first pixel storage capacitor***", "***the second pixel storage capacitor parallel connected to the first pixel storage capacitor***" and the relationship between the first pixel storage capacitor and the second pixel storage capacitor. In other words, Applicants thinks that the Examiner fails to establish prima facie obviousness of a claimed invention because not **all the claim limitations is taught or suggested by *Jang* and *Chae***.

For at least the foregoing reasons, Applicant respectfully submits that independent claims 1, 10, 20 and 22 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 2-9, 11-19 and 21 patently define over the prior art as well.

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CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1-22 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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